# A 250kHz, 500W Power Factor Correction Circuit Employing Zero Voltage Transitions

**James P. Noon**

## Introduction

The advantages and justification for power factor correction have been well documented.[1,2,3] High power factor converters reduce system power requirements, or more precisely, allow full use of the available source power. In some systems, twice as many power factor corrected converters as non-corrected converters can be connected to the line.

The most popular PFC topology is the boost converter operated in the continuous conduction mode. It offers several advantages over the buck and flyback topologies. The buck converter requires that the output voltage be lower than the input; which precludes obtaining high power factor due to the sinusoidal input voltage. The flyback converter suffers from a discontinuous input current that generates more EMI than an equivalent boost converter. In addition, the flyback switch ratings are greater than the boost.

Conversely, a fundamental property of the boost converter is a smooth input current waveform. This results in much less EMI and therefore reduced filtering requirements. The inductor current is the input current in a boost converter and is therefore easily programmed. For these reasons the boost converter, shown in Figure 1, is the most widely used topology for active power factor control.

While the boost converter works well in most applications, it too suffers from some potential problems. In order to maintain good EMI performance and reduced switch current ratings, the boost converter is usually operated in the continuous conduction mode (CCM). The disadvantage of CCM, however, is the increased stress on the boost diode. Referring to Figure 1, while the boost switch (Q), is off, load current flows through the boost diode D. When the switch turns on, the diode must recover quickly to prevent the output capacitor from discharging into the switch.

The diode has a finite reverse recovery time, trr, during which time it experiences reverse current through, and reverse voltage across it. Obviously this leads to increased power dissipation in the diode, which can be significant. Using faster diodes will help, however, hard turn-off of the diode also increases EMI. The nature of this effect makes it somewhat difficult to predict accurately and degrades diode reliability. In addition to the increased diode loss, the main switch experiences increased turn-on loss due to the reverse diode current. This increase in switching loss is accentuated as switching frequencies increase.

The trend in power converters is towards increasingly higher power densities. Usually, the method to achieve this is to increase the switching frequency, which allows a reduction in the filter component's size. The filter components can be the limiting factor in circuit volume since the control functions can be handled within a single IC and the power semiconductors are relatively small. Raising the switching frequency however, significantly increases the system

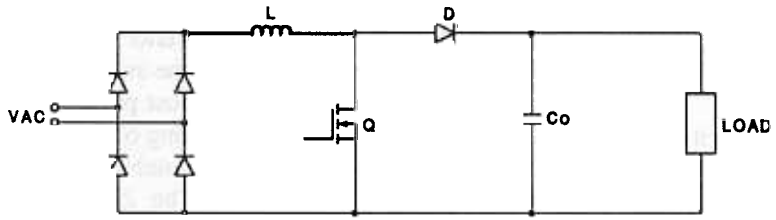


*Fig 1. - PFC Boost Converter*

switching losses which generally precludes operating at switching frequencies greater than 100kHz in high power factor applications.

In order to increase the switching frequency while maintaining acceptable efficiency, several soft switching techniques have been developed.[4,5,6] Most of these resonant techniques increase the semiconductor current and/or voltage stress, leading to larger devices and increased conduction losses due to greater circulating current. A new class of converters, however, allow an increase in switching frequency without the associated increase in switching losses, while overcoming most of the disadvantages of the resonant techniques.[7] Zero voltage transition (ZVT) converters operate at a fixed frequency while achieving zero voltage turn-on of the main switch and zero current turn-off of the boost diode. This is accomplished by employing resonant operation only during switch transitions. During the rest of the cycle, the resonant network is not functional, and converter operation is identical to its nonresonant counterpart.

## Design Overview

**PFC Fundamentals:** The function of a power factor correction circuit is to force the converter to look like a resistive load to the line. A resistive load has 0° phase displacement between its current and voltage waveforms (and no added harmonics). The standard definition of power factor is the ratio of real to apparent power. Real or average power is the product of the voltage and current magnitudes multiplied by the cosine of the angle between them, while apparent power is the product of the rms values.

$$PF = \frac{P}{V_{RMS}\, I_{RMS}}$$

When considering two sinusoidal waveforms with the same frequency, power factor can be defined in terms of the phase angle between them, i.e.:

$$PF = \cos \Theta$$

The power factor can be leading (capacitive) or lagging (inductive) depending on the angle between the voltage and current. This relationship only holds for two sinusoidal waveforms.

A switching converter's input current waveform is not sinusoidal; it has high harmonic content because it draws pulses of current at the peaks of the voltage waveform, if not power factor corrected. The measure of line distortion normally used is total harmonic distortion (THD), which is a measure of the harmonic content of a waveform. THD is given by:

$$THD = \sqrt{\frac{\sum_{n\neq 1} I_n^2}{I_1^2}}$$

THD and power factor are related since distortion increases the RMS current drawn from the line. It can be shown[8] that power factor and THD are directly related.

$$PF = \sqrt{\frac{1}{1+THD^2}}$$

This relationship should be kept in mind when specifying system performance or attempting to reduce THD or improve PF. A THD of 23% always results in a PF of 0.95; there is only one PF for a given THD.

Active power factor correction programs the input current of the converter to follow the line voltage and power factors of 0.999 with THD of 3% are possible. The Unitrode UC3855 IC incorporates power factor correction control circuitry capable of providing high power factor with several enhancements relating to current sensing and ZVT operation of the power stage.

**ZVT Boost Converter Power Stage:** This design will employ the ZVT boost converter with average current mode control. Average current ode control has been chosen for its ability to accurately program the input current while avoiding the slope compensation and poor noise immunity of other methods.[1,10] The ZVT boost converter operates the same as a conventional boost converter throughout its switching cycle except during the switch transitions. Figure 2 shows the ZVT boost power stage. The ZVT snubber network, consisting of $Q_{ZVT}$, D2, D3, $L_r$, and $C_r$, provides active snubbing of the boost diode and main switch. The ZVT circuit operation has been described in [7] and [9] and will

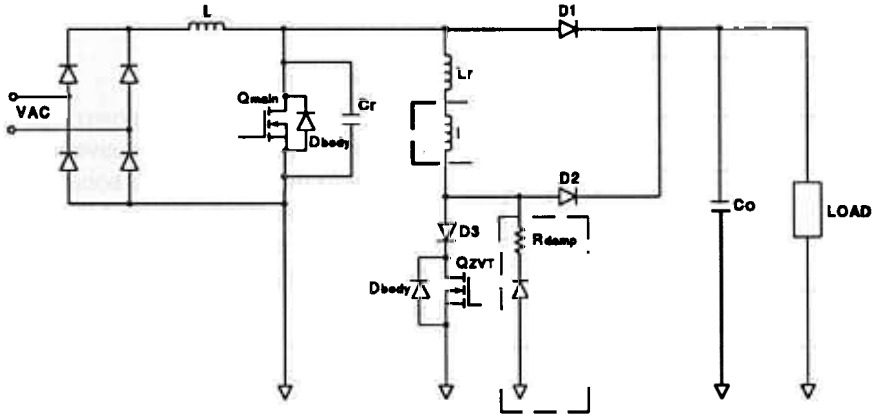


*Fig 2. - ZVT Power Stage*

be reviewed for completeness. Referring to Fig. 3, the following timing intervals are defined:

**t0 - t1:** During the time prior to t0, the main switch is off and diode D1 is conducting the inductor current. At t0, the auxiliary switch ($Q_{ZVT}$) is turned on. With the auxiliary switch ON, the current in $L_r$ ramps up linearly to $I_{in}$, while the current in diode D1 ramps down in a complementary manner. When the diode current reaches zero the diode turns off (i.e. soft switching of D1). Diode reverse recovery current can be quite small because of the relatively slow current transition caused by $L_r$. The voltage across the ZVT inductor equals $V_o$, therefore the time required to ramp up to $I_{in}$ is:

$$t_{01} = \frac{I_{in}}{V_o/L_r}$$

**t1 - t2:** At t1, the $L_r$ current has reached $I_{in}$ and $L_r$ and $C_r$ will begin to resonate. This resonant action discharges $C_r$ until its voltage equals zero. The dv/dt of the drain voltage is controlled by $C_r$ ($C_r$ is the combination of the external $C_{DS}$ and $C_{OSS}$). The current through $L_r$ continues to increase while $C_r$ discharges. The time required for the drain voltage to reach zero is 1/4 of the resonant period. The energy that was stored in $C_r$ has been transferred to $L_r$. At the end of this period the body diode of the main switch turns on.

$$t_{12} = \frac{\pi}{2}\sqrt{L_r C_r}$$

**t2 - t3:** At $t_2$, the switch drain voltage has reached 0 V and the body diode turns on. The current through the body diode is being driven by $L_r$. The voltage across the inductor is zero and therefore the current freewheels. The main switch should be turned on to achieve zero voltage switching as soon as possible after $t_2$.

**t3 - t4:** At t3, the UC3855 senses that the drain voltage of $Q_{Main}$ has fallen to zero and turns on the main switch while turning off the ZVT switch. After the ZVT switch turns off, the voltage across $L_r$ is clamped to $-V_o$, and the energy in $L_r$ is discharged linearly through D2 to the output.

**t4 - t5:** At t4, the current in D2 reaches zero. When this occurs, the circuit is operating like a conventional boost converter. In a practical circuit however, $L_r$ will ring with $C_{OSS}$ of the ZVT switch, driving the node at the anode of D2 negative (since the opposite end of $L_r$ is clamped to 0). This effect will be discussed in the ZVT circuit design section.

**t5 - t6:** This interval is also exactly like a conventional boost converter. The main switch turns off; node capacitance $C_r$ charges to $V_O$ and the main diode begins to supply current to the load. Since $C_r$ initially holds the drain voltage near zero while $Q_{MAIN}$ turns off, the turn off losses are minimal.

It can be seen through the above description that the operation of the converter differs from the conventional boost only during the turn-on switch transitions. The main power stage components experience no more voltage or current stress than normal and the switch and diode both experience soft switching transitions. Having significantly reduced the switching losses, the operating frequency can be increased without an efficiency penalty. This is important at higher power levels where

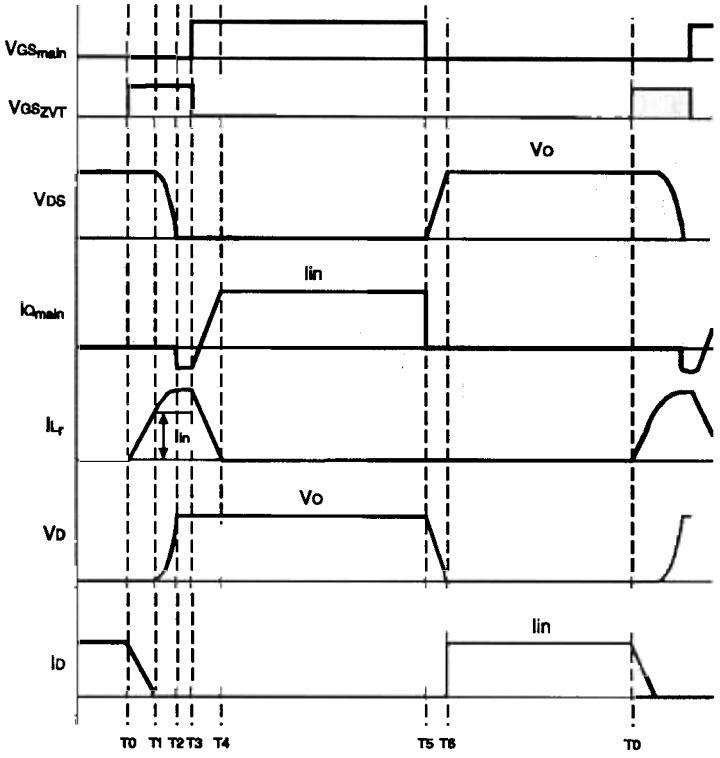


*Fig 3. - ZVT Timing Diagram*

losses can be severe. The diode also operates with much lower losses and therefore will operate at a lower temperature, increasing reliability. The soft switching transitions also reduce EMI, primarily caused by hard turn-off of the boost diode.

## Design Specifications

An example ZVT PFC boost converter was designed to the following specifications:

- **Vin = 85 - 270 VAC**
- **Vo = 410 VDC**
- **Po = 500W**
- **Fs = 250kHz**
- **Eff > 95%**
- **PF > 0.993**
- **THD < 12%**

The above specifications represent a common universal input voltage, medium power application. The switching frequency of 250kHz is now possible due to the soft switching, zero voltage transitions. The PF and THD numbers correspond to line correction achievable with the UC3855.

## Power Stage Design

**Inductor Design:** The power stage inductor design in a ZVT converter is identical to the conventional boost converter. The inductance required is determined by the amount of switching ripple current that can be tolerated. Allowing more ripple will reduce the inductor value, but this will increase input line noise and the peak current through the diode and switch. The worst case for peak current occurs at low line, maximum load. Peak power is equal to twice the average power and $V_{pk}$ is $\sqrt{2}\cdot V_{RMS}$. To calculate input current, an efficiency of 95% is assumed.

$$I_{pk} = \frac{2P_{in}}{\sqrt{2}\,V_{INmin}} = \frac{\sqrt{2}\left(\frac{500}{0.95}\right)}{85} = 8.7A$$

(60 Hz component)

A good compromise between current ripple and peak current is to allow a 20% p-p ripple to average ratio. This will also keep the peak switch current less than 10 A.

$$\Delta I = 0.2\,(8.7) = 1.7A_{pp}$$

Rearranging the conversion ratio for the boost converter to solve for D yields :

$$D = \frac{V_O - V_{in}}{V_O} = \frac{410 - \sqrt{2}\,(85)}{410} = 0.71$$

We can now calculate the required inductance.

$$L = \frac{V_{in}DT_S}{\Delta I} = \frac{\sqrt{2}\,(85)(0.71)4\mu s}{1.7} = 200\mu H$$

**Diode Selection:** Probably the most challenging component to choose in the boost converter is the boost diode, mainly due to the reverse recovery characteristics. A converter employing ZVT, however, benefits from soft switching of the diode. With ZVT, the boost diode has a negligible impact on

switching losses, and therefore a slower diode could potentially be used. However, there are still valid reasons for using an ultra fast diode in this application.

The ZVT inductance required is largely determined by the diode recovery time. A slower diode will require a larger $L_r$. This will require a correspondingly longer $Q_{ZVT}$ on-time, increasing conduction loss. A larger inductor will also require a longer time to discharge. To ensure complete discharge of the resonant inductor, the main switch minimum on-time should be approximately equal to the ZVT circuit on-time. This yields:

$$D_{min} = \frac{t_{01}+t_{12}+t_{rr}}{T}$$

$D_{min}$ effects the minimum allowable output voltage for the boost converter to continue operating. The ZVT circuit on-time is a strong function of $t_{rr}$, therefore choosing an ultra fast diode will keep the resonant circuit losses to a minimum and cause the least impact on the output voltage. The effective system duty cycle is primarily a function of the main switch on-time, since for a large portion of the resonant switch on-time, the voltage at the anode of the boost diode is held up by the resonant capacitor.

These considerations suggest a diode with a recovery time less than 75ns. The International Rectifier HFA15TB60 — a 15A, 600V ultrafast rectifier — is selected for this application. Average output current is less than 1.2A with a peak current of 9.2A. Diode conduction loss approximates 2.2W.

Using an ultrafast diode significantly reduces switching losses. This increases overall system efficiency and, perhaps even more importantly, reduces the peak stress of the diode and ZVT switch.

**MOSFET Selection:** The main MOSFET is chosen according to standard design criteria. The voltage rating must be sufficient to withstand the full output voltage. At low line, maximum load, the switch RMS current is approximately 8.7A. A 20A device provides the $R_{DS(on)}$ needed for an acceptable power dissipation. The Advanced Power Technologies APT5020BN is selected — rated at 500V, 23A, with $R_{DS(on)} = 0.20\Omega$ (25°C), Coss ≈ 500pF, in a TO-247 package.

It should be noted that the power loss within the MOSFET is mainly due to conduction loss. The turn-on losses are eliminated due to the ZVT operation. Turn-off losses are negligible due to the resonant capacitance which acts as a turn off snubber. $C_r$ directs current away from the switch at turn-off and transfers that energy to the inductor before turn-on, resulting in a significant loss reduction. Without ZVT, at 500W and 250kHz the switching losses can easily equal or exceed the conduction losses. In this example, the switching losses could exceed 25W without ZVT. The additional switching losses would require increased heat sink capacity and/or a larger package to operate with an equivalent junction temperature.

The UC3855's peak drive current capability of 1.5A is capable of driving the MOSFET without an additional drive stage. It should be noted that the drive requirements are relaxed due to the ZVT operation as the Miller capacitance effect is not an issue during turn-on since the drain is at 0V. Additionally, the turn-off dv/dt is limited by the resonant capacitor, reducing the possibility of inadvertent turn on due to insufficiently low drive circuit impedance.

**Output Capacitor Selection:** The selection criteria for the output capacitor is covered in detail in [12]. The value of the output capacitor impacts hold up time and ripple voltage. Since the ripple voltage is fed back through the voltage loop, excess ripple will require significant attenuation through the voltage error amplifier. This in turn will impair dc regulation. Hold up time is often the specification that determines capacitor value. Following the design approach outlined in [12], the output capacitor bank consists of two 820µF, 250V DC, capacitors in series for a combined voltage capability of 500V at 410µF.

## ZVT Circuit Design

**Resonant Inductor:** The ZVT circuit design is actually fairly straightforward. The circuit is performing an active snubber function and, as such, $L_r$ is designed to provide soft turn off of the diode while $C_r$ is selected to provide soft switching of the MOSFET.

The resonant inductor controls the di/dt of the diode by providing an alternate current path for the boost inductor current. When the ZVT switch turns on, the input current is diverted from the boost diode to the ZVT inductor. The inductor value can be calculated by determining how fast the diode can be turned off. The diode turn-off time is related to its reverse recovery time. Calculating an exact value for $L_r$ is difficult due to the variation in reverse recovery characteristics within the actual circuit as well as variations in how reverse recovery is specified from manufacturer to manufacturer. An example of circuit conditions effecting the reverse recovery is the natural snubbing action of the resonant capacitor, which limits the dv/dt seen at the anode of the diode. A good initial estimate is to allow the current through $L_r$ to ramp up to the diode current within three times the diode's specified reverse recovery time. One constraint on the maximum inductance value is its affect on the minimum duty cycle. As was shown in the diode selection section, the L-C time constant effects $D_{min}$ and therefore $Vo_{min}$. Making $L_r$ too large requires increased conduction time of the ZVT MOSFET, increasing the resonant circuit conduction losses. As the value of $L_r$ is reduced, the diode will experience more reverse recovery current, and the peak current through the $L_r$ and ZVT MOSFET will increase. As the peak current is increased the amount of energy stored in the inductor will also increase ($E = \frac{1}{2}LI^2$). This energy should be kept to a minimum in order to reduce the amount of parasitic ringing in this node at turn-off.

The reverse recovery of the diode is partially a function of its turn-off di/dt. If a controlled di/dt is assumed, the reverse recovery time can be estimated to be approximately 60ns. If the inductor limits the rise time to 180 ns ($3 \cdot t_{rr}$), the inductance can be calculated:

$$di/dt = \frac{I_{ip}}{3\,t_{rr}} = 53A/\mu s$$

$$L_r = \frac{V_o}{di/dt} = \frac{410}{53A/\mu s} = 7.7\mu H$$

The inductor design is limited by core loss and resultant temperature rise, not saturating flux density. This is due to the high AC current component and the relatively high operating frequency. A good design procedure is outlined in [13] and is beyond the scope of this review. Several points will be mentioned however. The core material should be a good high frequency, low loss material such as gapped ferrite or moly-permalloy powder (MPP). Powder iron cores will generally not be acceptable in this application. The less expensive Magnetics Kool Mu material, although exhibiting higher losses than the MPP material, can also be used. The higher loss material will actually tend to damp the resonant ringing at the turn off of the ZVT switch. The inductor winding construction is also optimized by keeping interwinding capacitance to a minimum. This reduces the node capacitance at turn off and reduces the amount of damping required.

The inductor current can by found by analyzing the resonant circuit formed by $L_r$ and $C_r$ and recognizing that the resonant cycle begins when the current reaches $I_{in}$:

$$I_{Lr} = I_{in} + \frac{V_o}{\sqrt{L_r/C_r}} \sin\omega t$$

where $\omega = \frac{}{\sqrt{L_r C_r}}$

The peak current then is equal to $I_{in}$ plus the output voltage divided by the resonant circuit's characteristic impedance. Decreasing $L_r$ or increasing $C_r$ will increase the peak current. The inductor was designed using a Magnetics Inc. MPP core 55209 with 33 turns for an inductance of 8 µH.

**Resonant Capacitor:** The resonant capacitor is sized to ensure a controlled dv/dt of the main switch. The effective resonant capacitor is the sum of the MOSFET capacitance and the external node capacitance. The APT5020 has approximately 500 pF of output capacitance, so an external capacitance of 500 pF was added across the device. This capacitor limits the dv/dt at turn-off and consequently reduces the Miller effect. In addition, it reduces turn-off losses since the switch current is

diverted to the capacitor. The capacitor must be a good high frequency capacitor, and low ESR and ESL are required. It must also be capable of handling the relatively large charging current at turn-off, so two good choices are polypropylene film or a ceramic capacitor.

This combination of L and C yields a resonant quarter cycle of:

$$\frac{\pi}{2}\sqrt{L_r C_r} = 130ns$$

At this point the resonant circuit's impact on the output voltage can be calculated. To ensure discharge of the resonant inductor at high line:

$$D_{\min} = \frac{t_{01}+t_{12}+t_{rr}}{T} \quad (1)$$

and for a boost converter:

$$V_{O\min} = \frac{Vin_{pk}}{1-D_{\min}} \quad (2)$$

Substituting (1) into (2) and solving for Vo:

$$V_{O\min} = \frac{L_r I_p + V_{ip} T}{T - t_{rr} - \frac{\pi}{2}\sqrt{L_r C_r}} \quad (3)$$

Equation (3) can be solved using the previously established values and yields a minimum output voltage of 405 V.

**Switch and Rectifier Selection:** The ZVT switch also experiences some turn-on loss due to the discharge of its own drain-to-source capacitance. However, it doesn't experience high current and voltage overlap since the turn-on current is limited by the resonant inductor. The switch does experience turn-off and conduction losses however. Although the peak switch current is actually higher than the main switch current, the duty cycle is small, keeping conduction losses low. The ZVT switch will be one or two die sizes smaller than the main switch due to the low average drain current. The ZVT switch on time is :

$$t_{ZVT} = \frac{I_{ip} L_r}{V_o} + \frac{\pi}{2}\sqrt{L_r C_r}$$

The peak ZVT switch current is equal to the peak ZVT inductor current. A conservative approximation of the switch RMS current is made by assuming a square wave signal. The RMS of the current is approximated by:

$$I_{RMS} = I_{Lrp}\sqrt{\frac{t_{ZVT}}{T}}$$

This results in a peak of approximately 14A at maximum load and maximum ZVT on-time, however, the RMS is only 3.9A. An appropriate device in this application is the International Rectifier IRF840 which is rated at 500V, 8.0A continuous, with $R_{DS(on)} = 0.85\Omega$ (25°C) in a TO-220 package.

The rectifiers needed for the ZVT circuit also experience relatively low RMS current. Diode D2 returns the energy stored in the $L_r$ to the load. It is essentially in parallel with D1. During the time D1 is conducting, a small percentage of output current will flow through D2 (if a saturable reactor is placed in series with $L_r$ no current will flow through D2). Since D2 was conducting prior to $Q_{ZVT}$ turning on, the diode will experience some reverse recovery loss. For these reasons D2 needs to be an ultra-fast recovery diode and is usually chosen to be of similar speed as D1. The diode selected for D2 is a Motorola MURH860; a 600V device with a $t_{rr} \approx 35ns$.

Diode D3 blocks current from flowing up through the $Q_{ZVT}$ body diode when the inductor resets. D3 sees the same peak and RMS current as the switch. D3 should be a fast recovery diode to decouple the drain to source capacitance of $Q_{ZVT}$ from $L_r$, otherwise energy stored in the $Q_{ZVT}$ capacitance will resonate with $L_r$ when the ZVT switch turns off. Minimizing this effect will reduce the amount of snubbing required at this node. The diode chosen here was the MUR460. This is a 600V, 4 amp device with $t_{rr} \approx 75ns$.

To summarize, both diodes in the ZVT circuit experience low RMS current. The main selection criteria in addition to the blocking voltage (in both cases equal to Vo) is reverse recovery time. Choosing devices with fast recovery times will reduce parasitic oscillations and reduce EMI.

**ZVT Snubber Circuit:** The ZVT circuit requires some method for damping the parasitic oscillations that occur after the ZVT inductor

current goes to zero. Figure 4a shows the ZVT inductor current and diode D2 anode voltage without adequate damping. The figure shows that as the inductor current begins to discharge ($Q_{ZVT}$ turns off) to the output, the anode voltage is at $V_{out}$ (since D2 is conducting). As the inductor current passes through zero, the voltage rings negative since the opposite end of the inductor is clamped to 0V through the main switch body diode. The anode voltage can easily ring negatively to twice the output voltage (because the D3 node capacitance reduces once D3 recovers). This increases the reverse voltage stress on the diode to 3 times the output voltage! Keeping the energy in the node capacitance to a minimum will reduce the ringing and using fast recovery diodes improves the circuit performance.

Several methods of damping this oscillation have been proposed.[7,9] In this circuit two methods, the saturable reactor and resistive damping were investigated. A 51Ω, 10W noninductive resistor was combined with 8 turns on a Toshiba saturable core SA14x8x4.5 to control the ringing. The resistive damping method prevents the node from oscillating. However, it does not prevent current from flowing in D2 while D1 is conducting. If current flows through D2 during this time it will experience reverse recovery current when $Q_{ZVT}$ turns on. Saturable reactor $L_s$ prevents this current flow due to its high impedance. $L_s$ also decouples $L_r$ from the node capacitance, which prevents the node from oscillating.

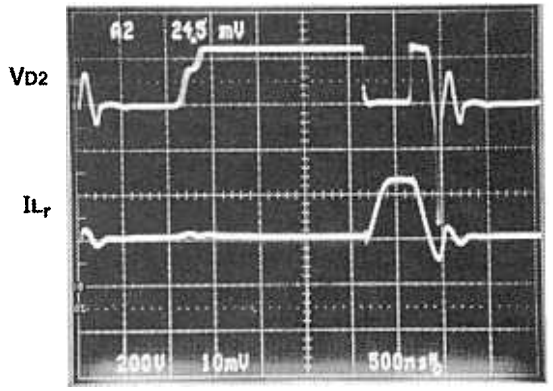


*Fig. 4a - Waveforms Without Damping*

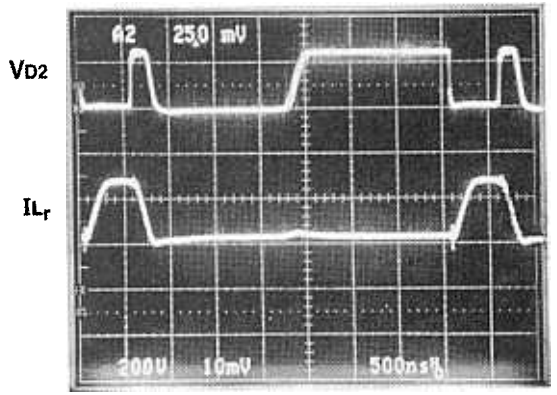


*Fig. 4b - Waveforms with Proper Damping*

The saturable reactor works well without the resistive damping and was the method chosen in this design. However, since $L_s$ is designed to saturate each switching cycle, the core loss is largely material dependent and can cause significant temperature rise of the core. In this circuit heatsinking of the core was required. An alternative design was also tried using the larger MS18x12x4.5 which ran cooler. Optimization of this circuit can significantly reduce the losses in the ZVT circuit. In this design, damping network losses were approximately 2W. Figure 4b shows the same circuit condition with the node damped with $L_s$.

## Control Circuit Design

Figure 5 shows the UC3855 controller block diagram. The UC3855 incorporates the basic PFC circuitry, including average current mode control, and the drive circuitry to facilitate ZVT operation. The IC also has current waveform synthesizer circuitry to simplify current sensing.

The oscillator contains an internal current source and sink and therefore only requires an external timing capacitor ($C_T$) to set the frequency. $C_T$ is calculated by:

$$C_T = \frac{1}{11200 f_s}$$

The UC3855 turns-off the ZVT drive signal (and turns-on the main switch) when the main switch drain voltage, sensed by the ZVS pin, falls below 2.5V. The network used to sense the node voltage is shown in Fig. 9. It consist of D6, C6 and R12. R12 is needed to pull pin 13 up in order to reset

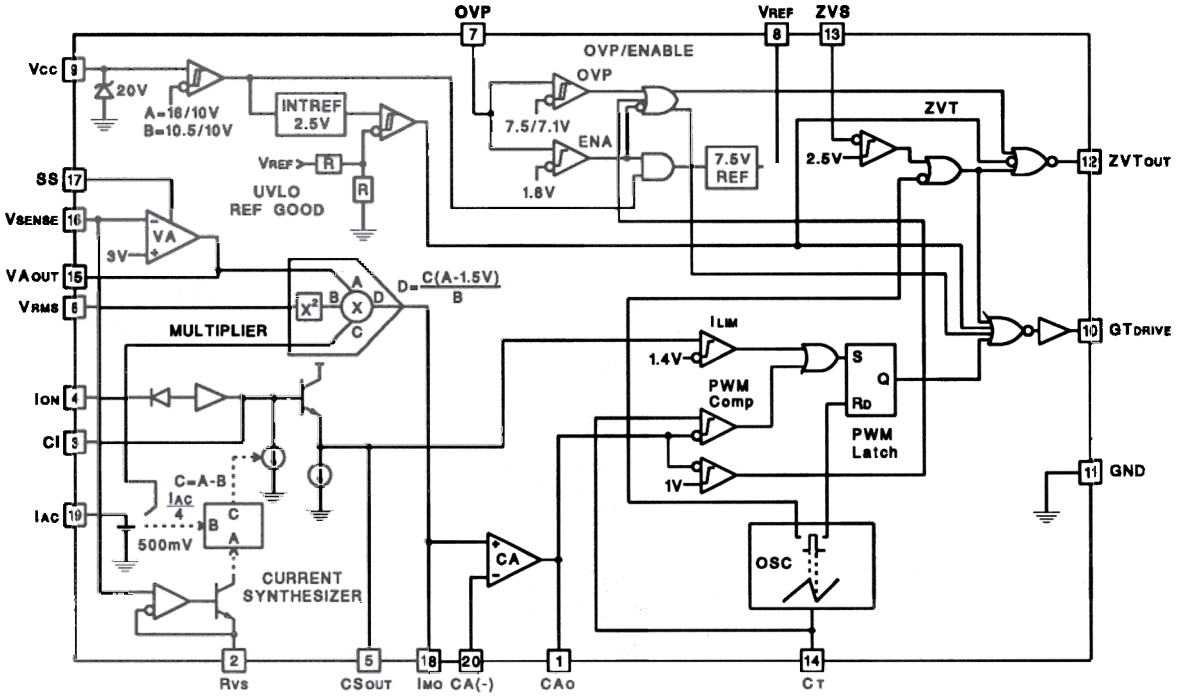


*Fig 5. - UC3855 Block Diagram*

the ZVS pin. The R12, C6 time constant should be short enough to allow charging above 2.5V at maximum duty cycle. Of course the drain voltage dv/dt is limited by the node capacitance. The components chosen in this application are C6 = 1000pF and R12 = 1kΩ. The ZVS pin voltage should not exceed $V_{REF}$, otherwise the IC can become latched and will not operate properly.

An alternative method for ZVS is to sense the node voltage through a simple voltage divider. This voltage will still have to be filtered however, so as not to inject noise into the ZVS pin.

The UC3855 also combines the enable and OVP function into one pin (pin 7). It requires a minimum of 1.8 V to enable the IC, and below this voltage, the reference is held low and the oscillator is disabled. A voltage above 7.5 V will interrupt the gate drive. The resistor divider should be sized for 7.5V when an over voltage condition is reached, this will allow start up at a reasonable line voltage.

**Multiplier / Divider Circuit:** The multiplier / divider circuit is programmed by determining the system power limits. Referring to Fig. 5, the multiplier output equation is:

$$I_{mo} = \frac{I_{AC}(V_{EA}-1.5)}{V_{RMS}^2}$$

Internally the multiplier output current ($I_{mo}$) is limited to 2 times $I_{AC}$. The power limit function is set by the maximum output voltage of the voltage loop error amplifier $V_{EA}$. The maximum output voltage available from the amplifier is 6V. The power limiting function is easily explained by looking at what happens for a given value of $V_{EA}$. If the AC line decreases by a factor of 2, the feedforward voltage decreases by one fourth. This increases multiplier output current (and therefore line current) by two. The power drawn from the line has therefore remained constant. It can be seen then that $V_{EA}$ is a voltage proportional to input power.

Normally the multiplier is set to limit maximum power at low line, corresponding to maximum error amplifier output voltage. The multiplier equation can be solved for the feedforward voltage that

corresponds to maximum error amplifier voltage and maximum multiplier current (which recall is limited to 2 times $I_{AC}$).

$$V_{RMS}^2 = \frac{I_{AC}(V_{EA} - 1.5)}{2(I_{AC})}$$

$$V_{RMS} = .5\ V$$

Knowing the $V_{RMS}$ voltage at low line defines the voltage divider from the line to pin 6. At a high line of 270V, this will correspond to $V_{RMS} = 4.7V$. The common mode range of pin 6 is 0 to 5.5V. The calculated range is therefore within the accepted limits.

Referring to Fig. 6 the components correspond to R9A = R9B = 300kΩ, R10 = 120kΩ, R11 = 13kΩ.

The value of $I_{AC}$ is chosen to be 500µA at high line. This value is somewhat arbitrary, however it should be kept below 1 mA to stay within the linear region of the multiplier. This corresponds to a total resistance of 766kΩ from the line to $I_{AC}$ (pin 19).

The UC3855 also has pulse by pulse current limiting. The multiplier power limit determines the maximum average power drawn from the line. However during transients or overload conditions a peak current limiting function is necessary. This function is implemented by sensing the switch current and feeding this value to a current limiting comparator that terminates the gate drive signal.

The multiplier output resistor can be calculated by recognizing that at low line and maximum load current, the multiplier output voltage will equal 1 V. This will correspond to the maximum sense voltage of the current transformer. The multiplier current is equal to 1V / $R_{IMO}$, and can be equated with the multiplier equation which yields:

$$\frac{1V}{R_{IMO}} = \frac{I_{AC}(V_{EA} - 1.5)}{V_{RMS}^2}$$

At low line $I_{AC}$ will equal 156µA (if low line = 85V and $I_{AC}$ was set to 500µA at 270V), $V_{EA}$ will be at its maximum of 6V, and $V_{RMS}$ will be 1.5V. Therefore $R_{IMO}$ equals 3.2kΩ.

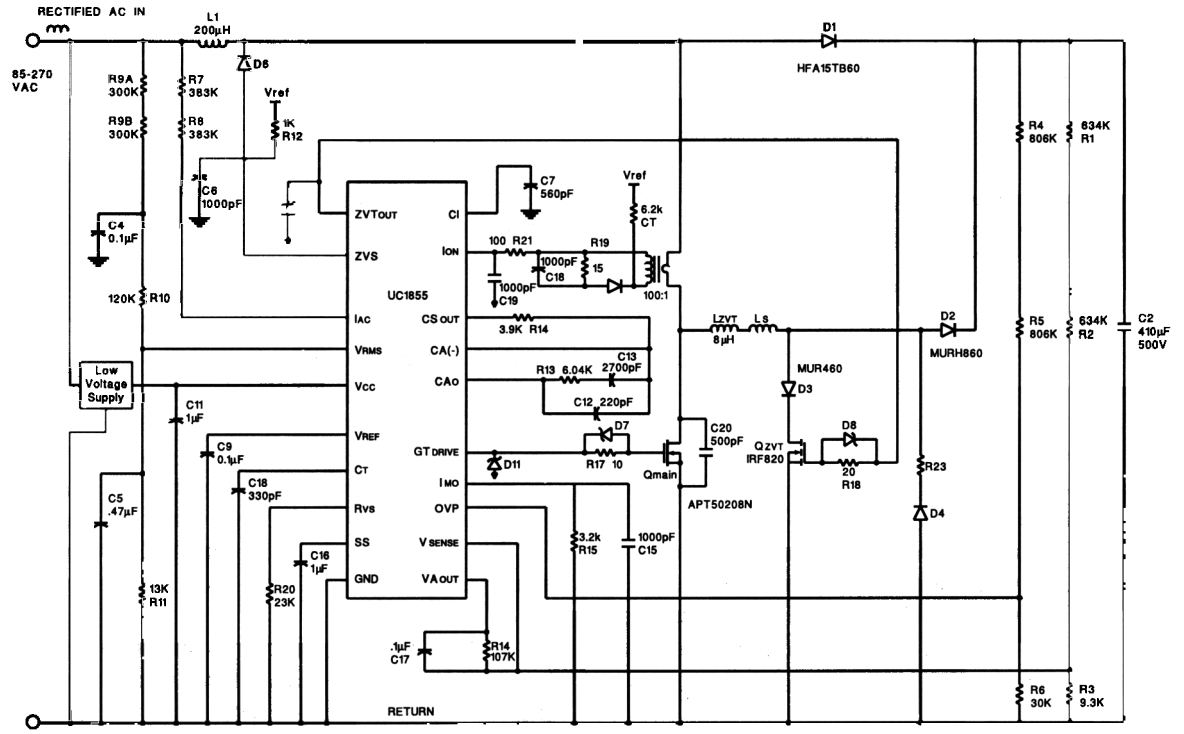


*Fig 6. - UC1855 PFC with ZVT Schematic*

**Current Synthesizer:** Current sensing is simplified due to the current synthesis function built into the UC3855. Switch current is the same as inductor current when the switch is on and can be sensed using a single current transformer. The current synthesizer charges a capacitor ($C_I$) with a current proportional to the switch current when the switch is on. During the switch off-time, the inductor current waveform is reconstructed by the controller. To get an accurate measure of the inductor current then, all that is required is to reconstruct the down slope of the inductor current, which is given by:

$$\frac{\Delta i}{\Delta t} = \frac{V_{out} - V_{AC}}{L}$$

Discharging $C_I$ with a current proportional to $V_{out}-V_{AC}$ will allow reconstruction of the inductor current waveform. The capacitor down slope is:

$$\frac{\Delta v}{\Delta t} = \frac{I_{DIS}}{C_I}$$

The UC3855 develops $I_{DIS}$ by subtracting $I_{AC}/4$, from a current proportional to $V_{out}$. The current proportional to $V_{out}$ is derived by the current through $R_{VS}$. $V_{out}$ is regulated to 3V at $V_{SENSE}$; this voltage also appears at the $R_{VS}$ pin. Equating inductor current slope with capacitor voltage slope, and recognizing that maximum slope occurs when $V_{AC}$ equals zero, $C_I$ can be solved by:

$$C_I = \frac{3LN}{R_{VS} V_{OUT} R_S}$$

where N is the current transformer (CT) turns ratio, (Ns / Np) and $R_S$ is the current sense resistor.

$R_{VS}$ is sized by setting the synthesizer current to 130µA. This is based on the discharge time available at high line. Setting $I_{RVS}$ to 130µA gives a 5µA discharge current at high line (this corresponds to 6% of maximum charge current, which corresponds to the switch duty cycle at high line).

$$R_{VS} = \frac{3V}{130\mu A} = 23\,K\Omega$$

If N is chosen to be 100 then the sense resistor will be 10.5Ω. Solving the above equation results in $C_I$ = 560pF.

**Current Sensing:** As was seen in the previous section, synthesizing inductor current with the UC3855 is quite simple. Only switch current needs to be sensed directly, and this is most efficiently done with a current sense transformer. Resistive sensing at this power level would result in excessive power dissipation.

The current transformer is designed to produce 1V at peak input current. This allows sufficient margin before the current limit trip point (1.4V) is reached. A turns ratio of 100:1 will keep the sense network losses less than 150mW and allow the use of a 1/4 Watt resistor. Solving for the sense resistor yields:

$$R_S = \frac{1V}{I_{SW}/N} = \frac{1V}{9.5/100} = 10.5\,\Omega$$

Several issues should be kept in mind when implementing the CT. At frequencies of a couple hundred kilohertz, core reset needs to be addressed. Contributing to the difficulty is the very high duty cycles inherent in a power factor correction circuit. In this type of application, active transformer reset methods should be considered. Figure 7 shows the method used in this design. The circuit operates like a normal CT when switch current is flowing. When switch current is interrupted, a DC current is forced through the resistor and the secondary windings. This charges the parasitic capacitance much quicker than the transformer's magnetizing current alone would, and resets the transformer. This method is further discussed in Unitrode Design note DN-41. Keep in mind that the resistor should be sized to

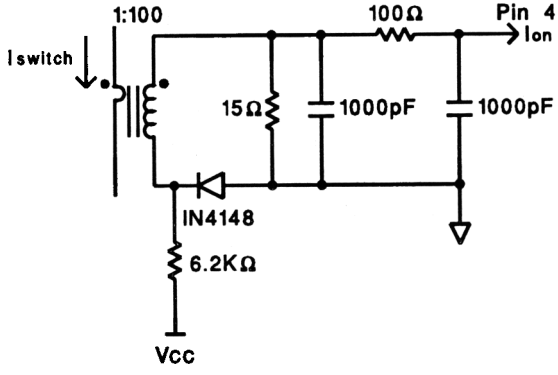


*Fig 7. - Current Transformer with Reset*

minimize the error term when switch current is flowing. This method also tends to damp the transformer at turn off which reduces noise coupling to the current sense pin of the IC.

Figure 7 also shows that a capacitor is added to the transformer secondary in order to provide noise filtering. The bandwidth of this filter should be low enough to reduce switching noise without degrading the switch current waveform.

**Small Signal Model:** The small signal model of the ZVT PFC boost converter is similar to the standard PFC boost converter model. The two converters operate exactly the same throughout most of the switching cycle. Only during switching transitions is there any difference. This allows the design of the control loops to proceed following the standard techniques outlined in [12].

**Current Loop Design:** Excellent references on the current loop design are found in [1,12,14]. The design of the average current mode control loop begins with choosing a crossover frequency. In this example the switching frequency is 250kHz so the unity gain crossover frequency could be chosen to be as high as 40kHz. In this circuit however, the crossover is chosen to be 10kHz. Since the main job of the current loop is to track the line current, a 10kHz bandwidth is quite adequate for this application.

Once the crossover frequency, *fc*, is known, the next thing to do is calculate the gain of the power stage. The small signal model of the power stage including the current sense network is given below. This model does not include the sampling effect at one half the switching frequency[15] but is a good approximation at the frequencies of interest.

$$G_{id}(s) = \frac{V_O R_{sense}}{s L V_{SE}}$$

The UC3855 has an oscillator ramp of 5.2Vpp ($V_{SE}$). The $R_{sense}$ term is the attenuation from actual input current to sensed current (i.e. it includes the CT turns ratio). Using the previously determined component values and solving for the power stage gain at $f_c$ yields a gain of 0.66 at 10kHz. In order to have a gain of 1 at $f_c$, the error amplifier must have a gain of 1/.66 at 10kHz. The error amplifier is shown in Figure 8a with the frequency response in Fig. 8b. The resistor Ri is equal to 4kΩ so the feedback resistor is chosen to be 6.04kΩ. A zero is placed at the crossover frequency to give a phase margin of 45 degrees. To reduce switching noise a pole is placed at one-half the switching frequency. The following summarizes the design procedure.

$$|G_{id}(s)| = \frac{410V \cdot .105}{2\pi \cdot 10kHz \cdot 200\mu H \cdot 5.2} = 0.66 \quad (1)$$

$$G_{EA} = \frac{1}{|G_{id}(s)|} = 0.66 \Rightarrow A_V = \frac{R_f}{R_i}$$

$$\therefore \quad R_f = \frac{1}{|G_{id}(s)|} \approx 6.04\,k\Omega \quad (2)$$

$$f_z = f_c = \frac{1}{2\pi R_f C_z}$$

$$C_Z = \frac{1}{2\pi \cdot 10kHz \cdot 6.04k\Omega} \approx 2700pF \quad (3)$$

$$f_p = \frac{}{2\pi R_f \left(\frac{C_z C_p}{C_z + C_p}\right)} \approx \frac{1}{2\pi R_f C_p}$$

$$C_p = \frac{1}{2\pi \cdot 6.04k\Omega \cdot 125kHz} \approx 220pF$$

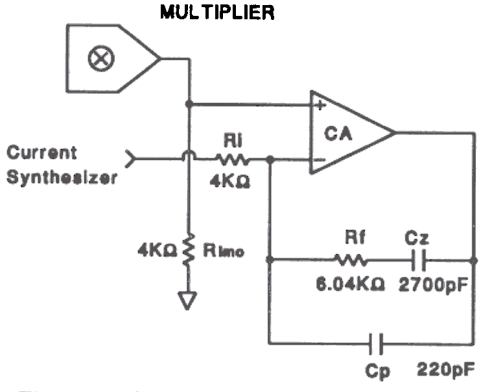


*Fig. 8a - Current Loop Error Amplifier*

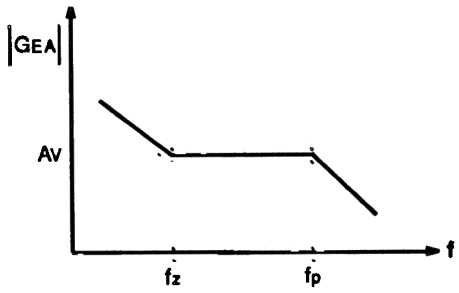


*Fig. 8b - Current Amplifier Gain Plot*

**Voltage Loop Design:** The design of the voltage loop follows the procedure given in [1]. The first step is to determine the amount of ripple on the output capacitor.

$$v_{Opk} = \frac{P_{IN} X_{Co}}{V_O}$$

$$v_{Opk} = \frac{525}{2\pi \cdot 120 \cdot 410\mu \cdot 410} = 4.14\,V_{pk} = 8.3\,V_{pp}$$

In order to meet the 3% THD specification, the distortion due to output ripple voltage feeding through the voltage error amplifier will be limited to 0.75%. This allows 1.5% from the multiplier and 0.75% from miscellaneous sources. A 1.5% second harmonic on the error amplifier will result in 0.75% 3rd harmonic distortion at the input. At full load, the peak error amplifier ripple voltage allowed is:

$$v_{EApk} = \%ripple\,(V_{VEA}) = 0.015\,(6-1) = 0.075\,V$$

The error amplifier gain at 120 Hz is the allowable error amplifier ripple voltage divided by the output ripple voltage, or 0.009 (-41dB). The error amplifier input resistor was chosen to be 1.26MΩ to keep power dissipation low and allow a small value for the compensation capacitor. Two 634kΩ resistors in series are used to reduce the voltage stress. The voltage error amplifier schematic is shown in Fig. 9a, with the 120Hz gain determined by the integrator function of $C_f$ and $R_i$. This network has a single pole roll off and the capacitor value is easily found to give the desired gain at 120Hz.

$$C_f = \frac{1}{2\pi f\, G_{VEA} R_i}$$

$$C_f = \frac{1}{2\pi \cdot 120 \cdot 0.009 \cdot 1.25M} = 118\,nF \quad (use\,0.1\mu F)$$

The crossover frequency can now be calculated recognizing that a pole (due to the combination of $C_f$ and $R_f$) will be placed at the crossover frequency to provide adequate phase margin. The pole placement will determine the phase margin since the power stage has a single pole response with the associated 90 degree phase lag. If the error amplifier pole is placed at the crossover frequency, the overall loop gain will have a 45 degree phase margin. The power stage gain is given by:

$$G_{ps}(s) = \frac{v_O}{v_{VEA}} = \frac{P_{IN}}{\Delta V_{EA} \cdot V_O \cdot sC_O}$$

The voltage loop gain (T) is the product of the power stage gain and the error amplifier gain. To find the crossover frequency, solve for f and set equal to 1.

$$T = \quad = G_{PS}\, G_{VEA}$$

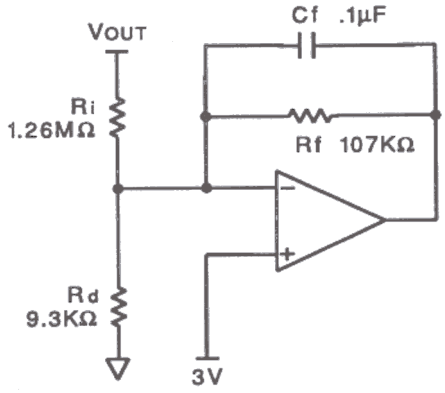


*Fig. 9a - Voltage Loop Error Amplifier*

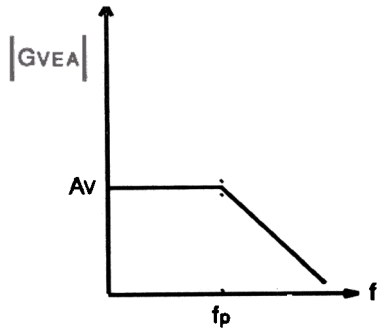


*Fig. 9b Voltage Amplifier Gain Plot*

The error amplifier gain is:

$$G_{VEA} = \frac{-j}{2\pi f R_I C_f} = \frac{-j2.25}{f}$$

$$\therefore \quad T = 1 = \frac{-j99.4}{f}\left(\frac{-j2.25}{f}\right) = \frac{223}{f^2}$$

The crossover frequency then is 15 Hz, so the resistor, $R_f$, can be calculated to place the pole at $f_c$.

$$R_f = \frac{1}{2\pi \cdot 15 \cdot 0.1\mu} \approx 107\text{k}\Omega$$

Finally, the resistor $R_D$ (9.3kΩ) sets the DC output voltage to 410 V.

## Experimental Results

The example converter was constructed to demonstrate circuit performance. The circuit performed well and was tested over the full line and load ranges. At this stage circuit testing concentrated on the ZVT operation.

Figure 10 shows efficiency data for the ZVT and a conventional boost converter, which was derived by simply removing the ZVT components. The conventional circuit was cooled with a fan in order to stabilize the power semiconductor temperatures. It can be seen from the data that the ZVT circuit has a significant advantage over the conventional converter at low line. At higher line voltages the advantage is reduced until the two power stages converge at high line. This is understandable and consistent with the other reported data.[7,11] At low line, the higher input current contributes to higher switching losses in the conventional converter. The ZVT converter however, does not experience increased switching losses (conduction losses increase for both converters).

Figure 11 shows the ZVT and main switch gate drives as well as the main switch drain to source voltage. The ZVT gate drive goes high prior to the

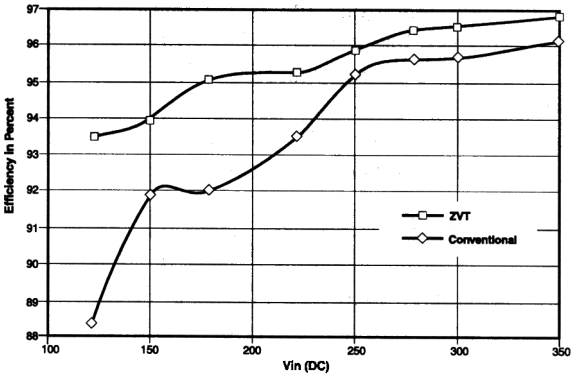


*Fig 10. - Efficiency vs. Input Voltage*

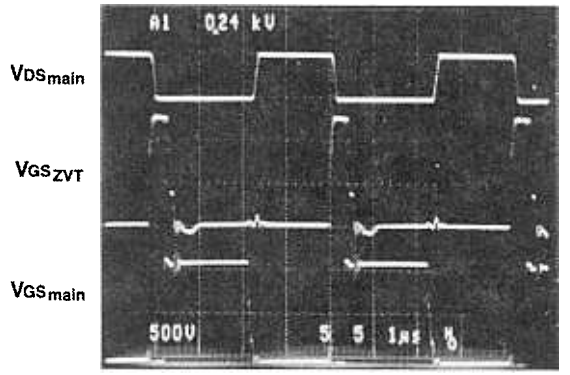


*Fig 11. - Power Stage Waveforms*

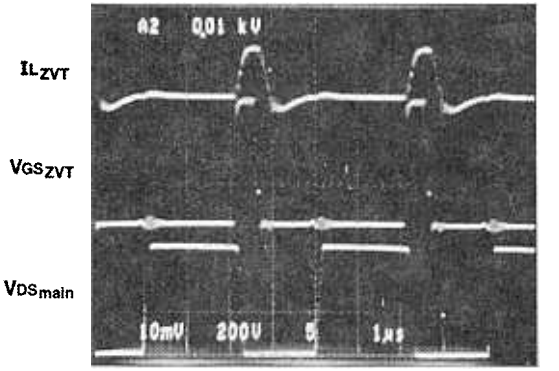


*Fig 12. - ZVT Waveforms*

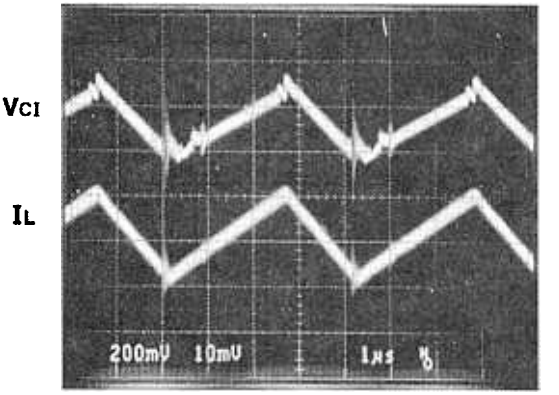


*Fig 13. - Current Synthesizer Waveforms*

main switch and drives the drain voltage to zero before the main switch turns on. It should also be noted that the drain to source voltage waveform is very clean with no overshoot or ringing, which will reduce EMI and voltage stress on the device. The ZVT circuit waveforms are shown in Figure 12. Current in $L_r$ is shown in the top trace. The waveforms are well damped with a peak current of approximately 6A. The current synthesizer waveforms are shown in Figure 13. The top waveform is the reconstructed waveform at $C_I$ and the bottom waveform is inductor current. The waveforms show good agreement. Any error between the reconstructed and actual waveform will be greatest at high line and is primarily caused by slight offset voltage errors in the synthesizer circuit.

## Conclusions

A ZVT PFC boost converter design example has been reviewed. Practical design equations for the boost stage and control IC have been presented. Circuit operation has been verified and a working model built and tested. The Zero Voltage Transition technique appears to have great promise. It allows an increase in switching frequency while reducing EMI and switching losses and reducing diode stress. The technique reduces switching loss without increasing voltage or current stress in the power stage components. This is the main advantage with the ZVT technique over traditional resonant converters or passive clamp designs.

The efficiency improvements over the conventional boost converter are significant at low line. At even higher power levels this will translate into significant thermal improvements. In addition, the decreased stress on the boost diode and switch, due to the reduction in reverse recovery current, contributes to increased reliability and reduced EMI. These benefits would seem to offset the increased complexity.

The UC3855 provides an integrated control solution combining ZVT power stage operation with active PFC. Additionally, the UC3855 incorporates the current synthesizer function to greatly simplify control circuit design. Further development work into system trade-offs and optimization is ongoing at Unitrode Integrated Circuits.


## Acknowledgments:

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## Power Stage Component Vendors:

| | |
|---|---|
| L1,L2 | Magnetics, Butler, PA (412) 282-8282 |
| Spike Killer | Toshiba, Westboro, MA (508) 836-3939 |
| $Q_{main}$ | APT, Bend, OR (503) 382-8028 |
| $Q_{ZVT}$, D1 | International Rectifier, El Segundo, CA (310) 322-3331 |
| D2, D3, D4 | Motorola, Phoenix, AZ (602) 244-3550 |

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